

FIG. 1 is a block diagram of a baseband processor 100 according to one embodiment of the present invention.

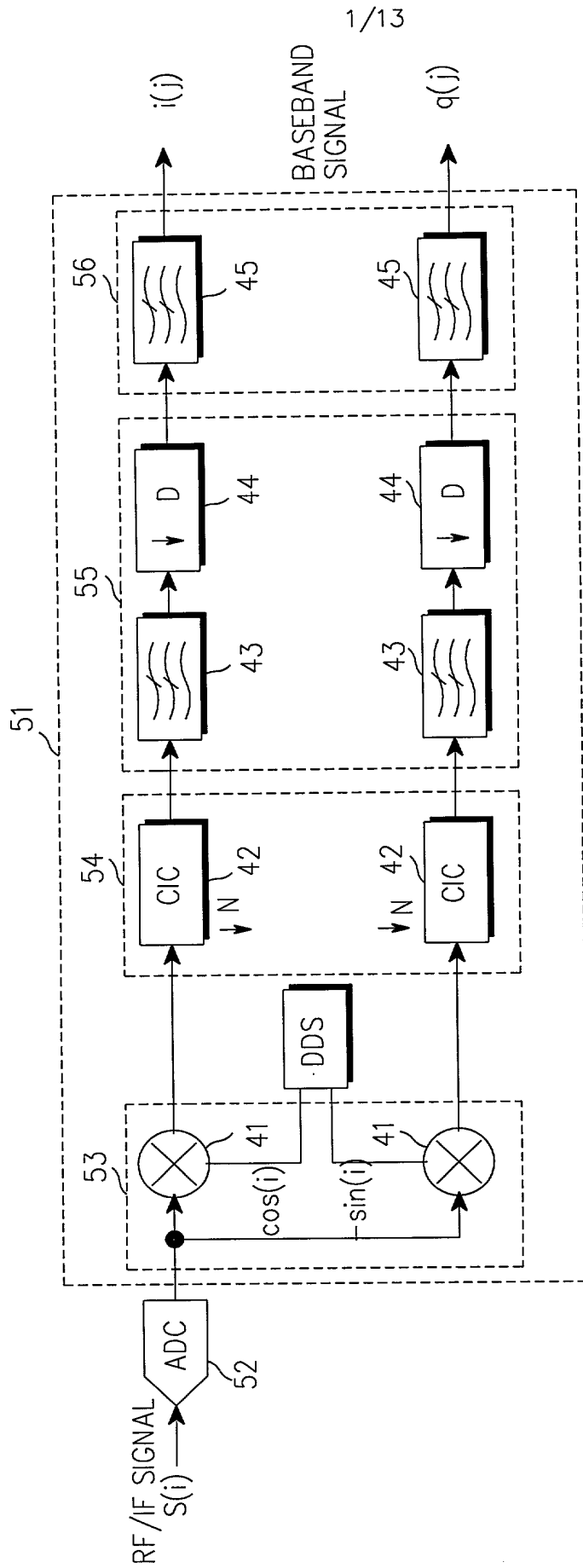


FIG. 1  
(PRIOR ART)

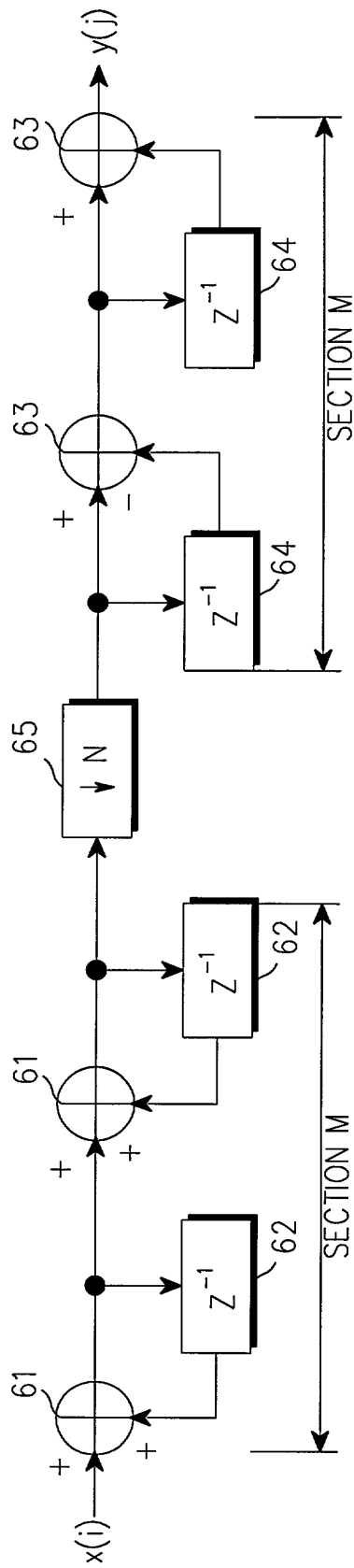
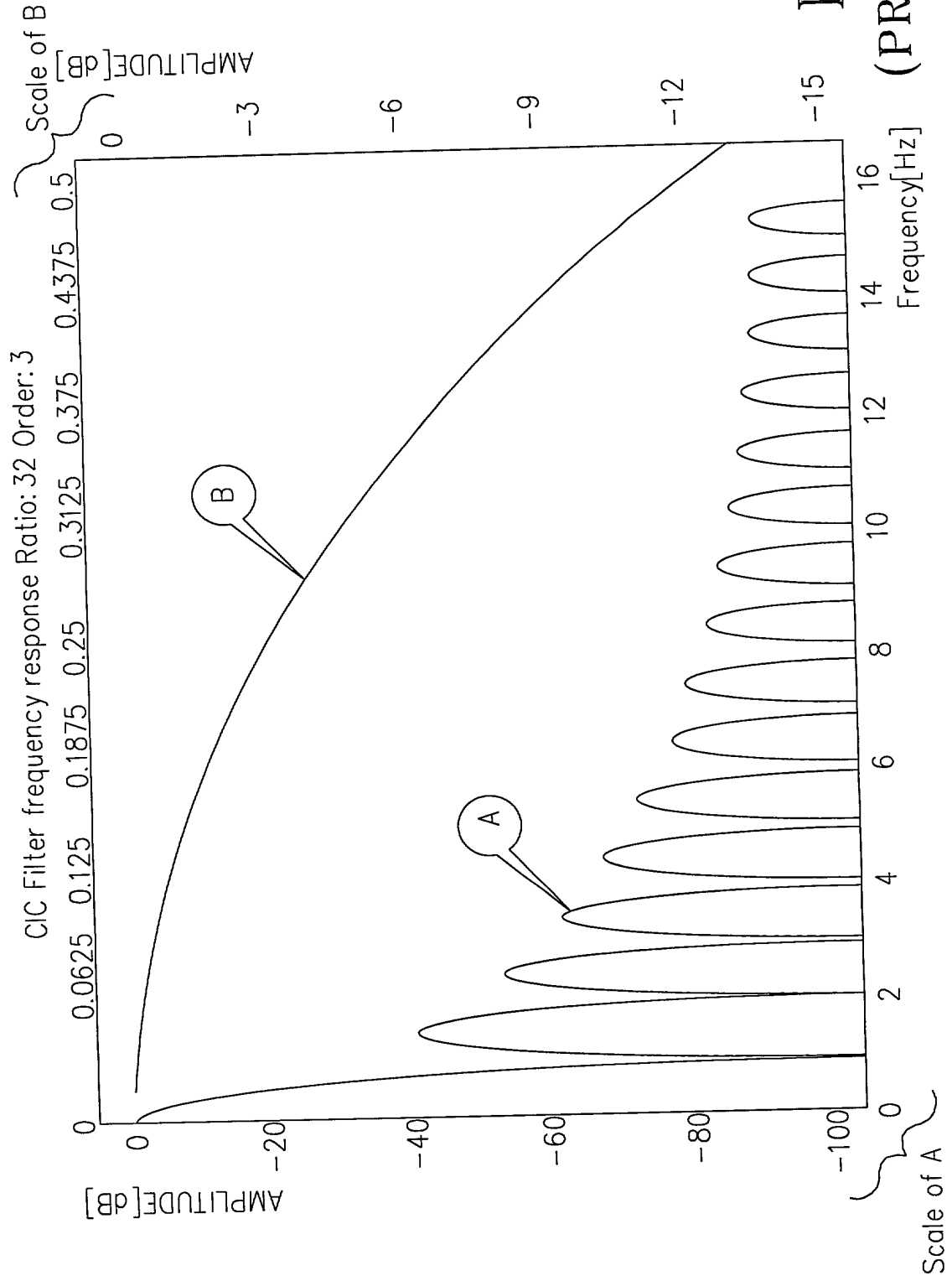


FIG. 2  
(PRIOR ART)



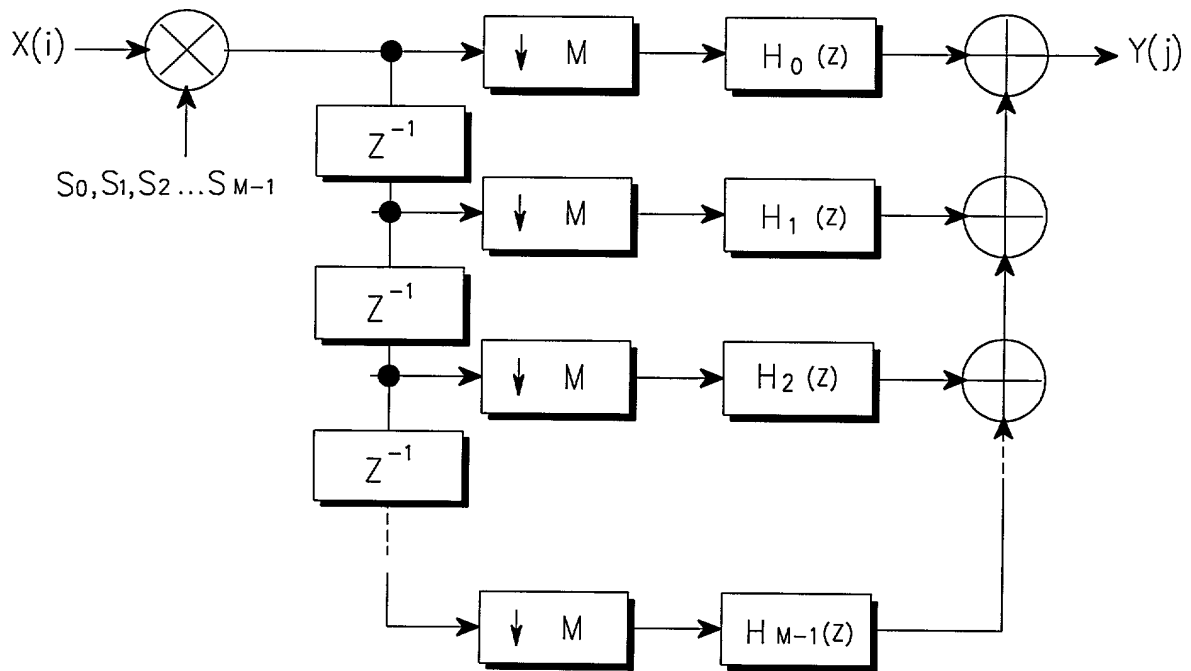


FIG. 4A

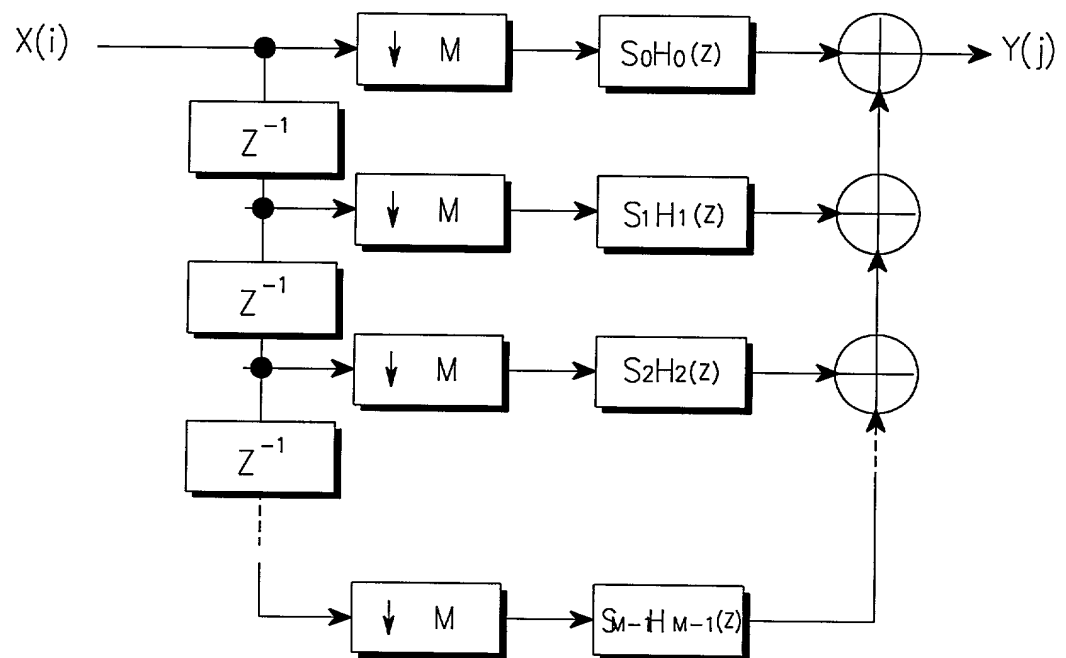


FIG. 4B

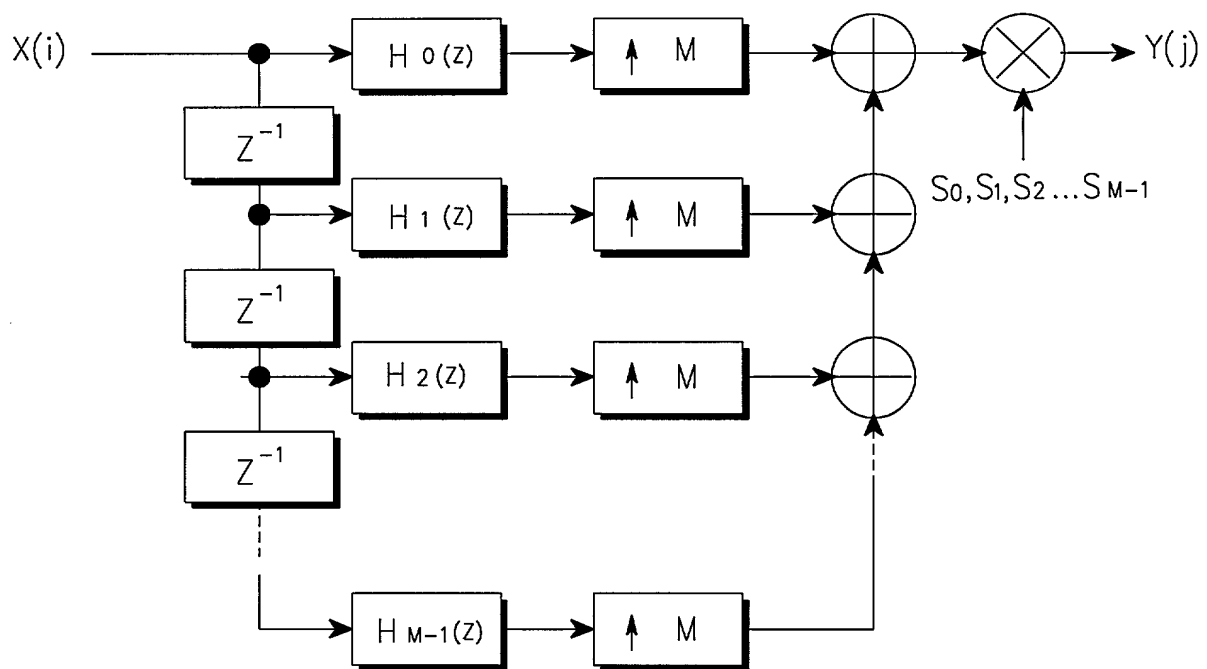


FIG. 5A

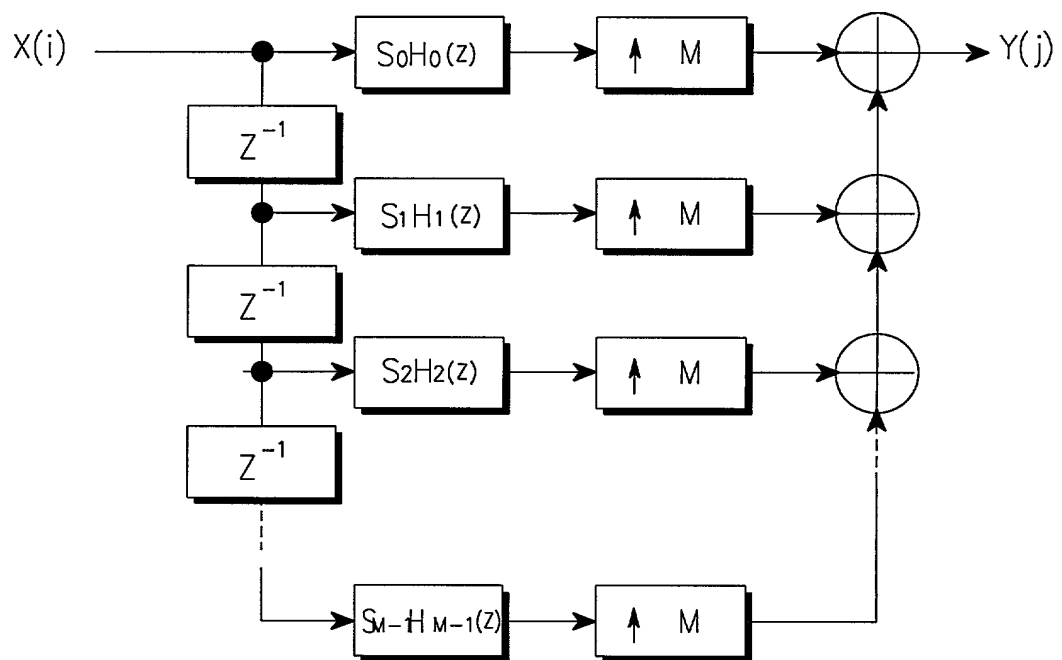


FIG. 5B

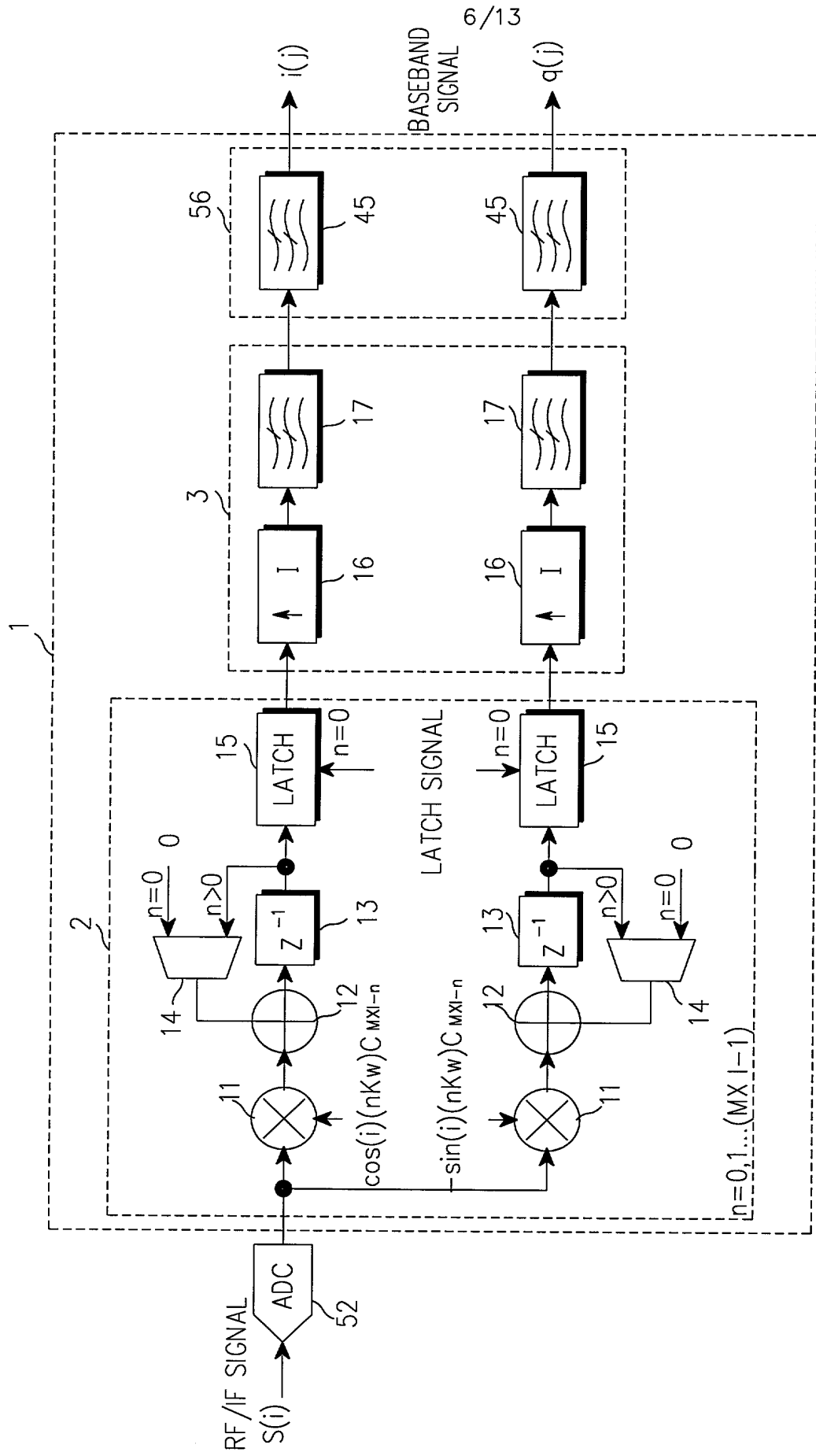


FIG. 6

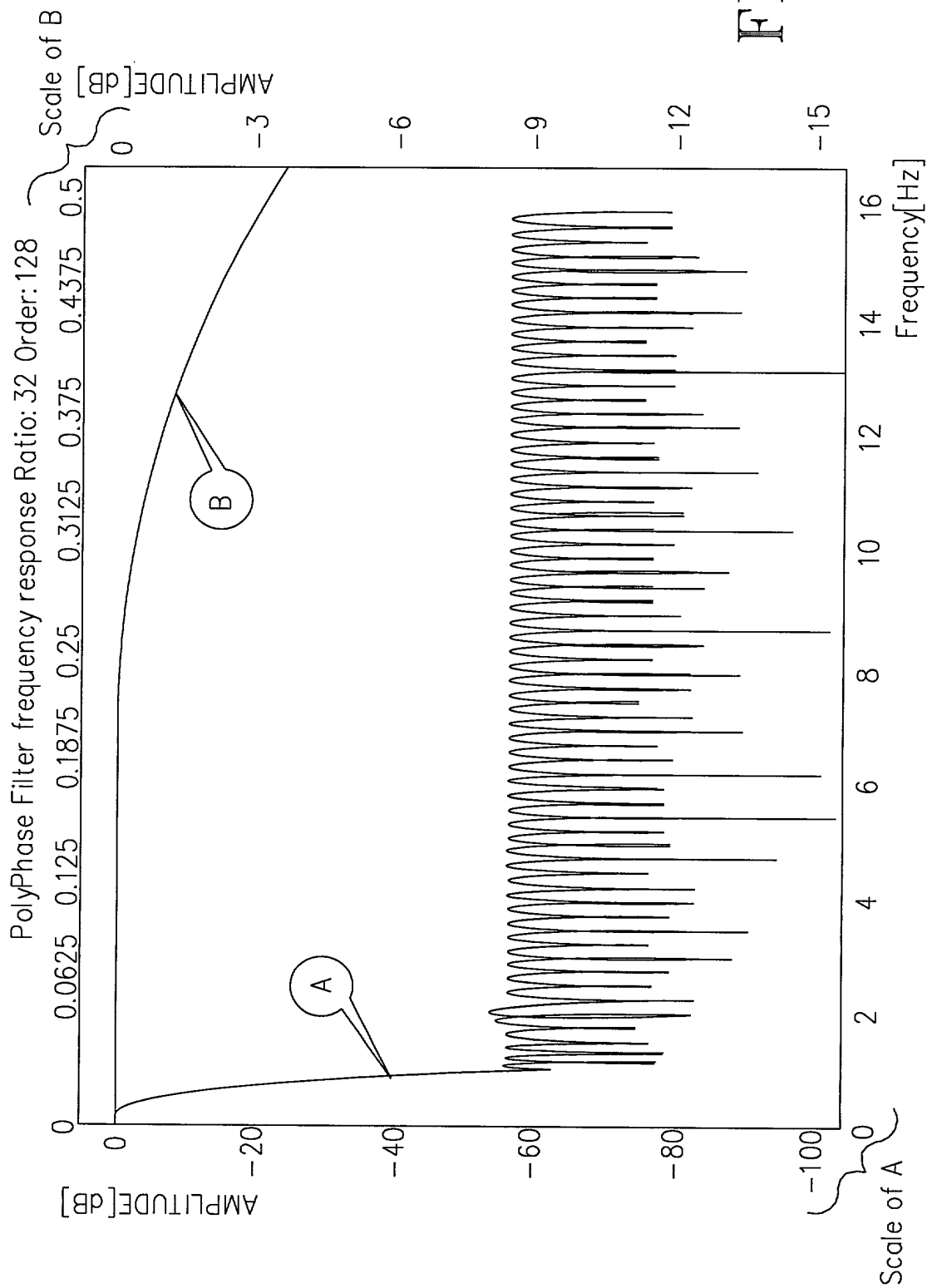


FIG. 7

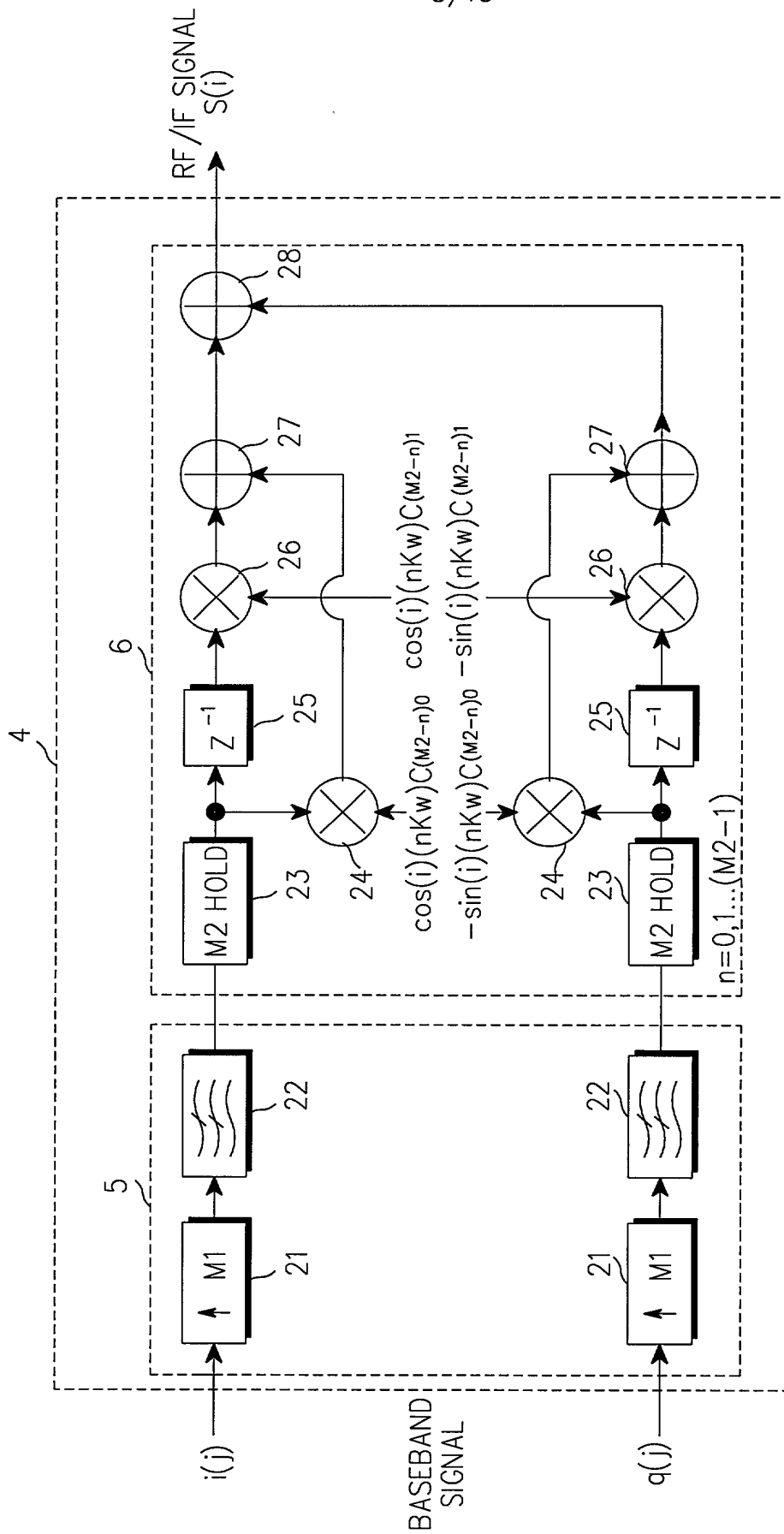


FIG. 8



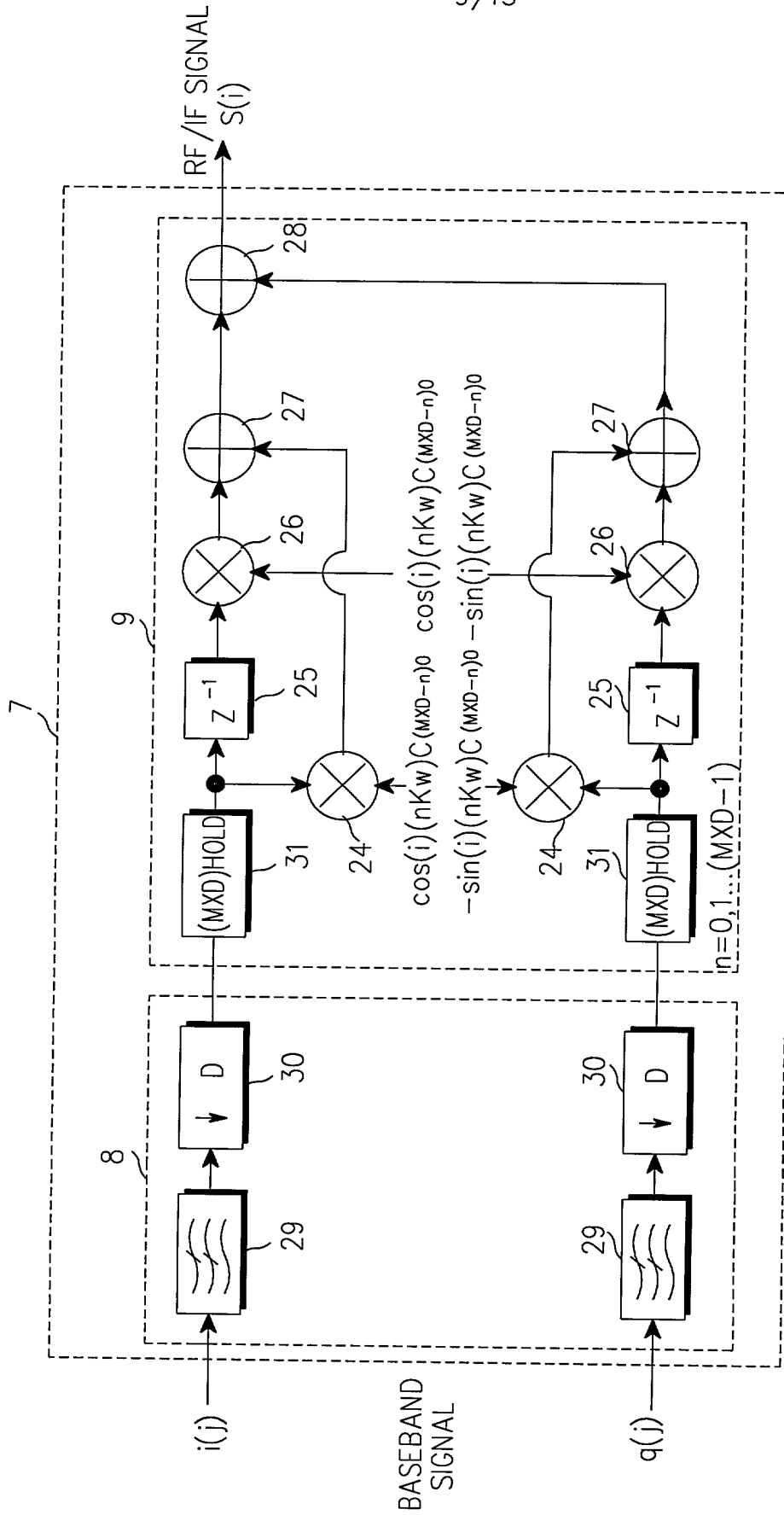
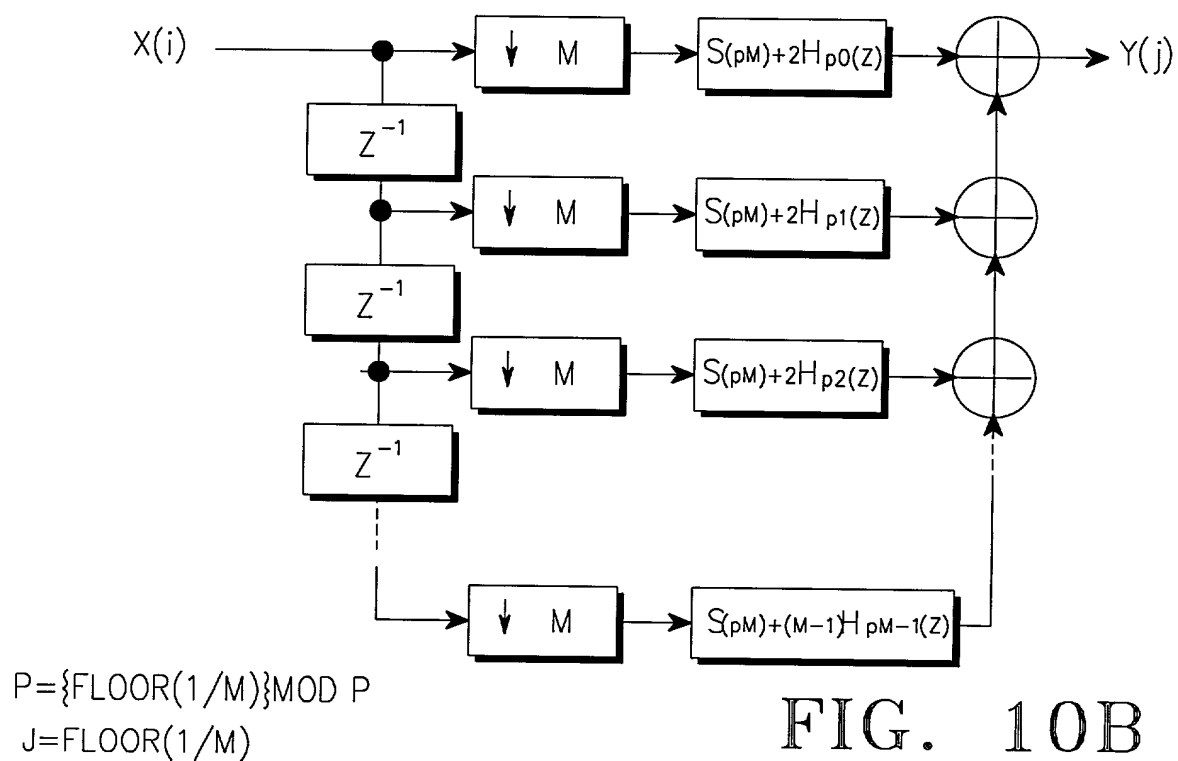
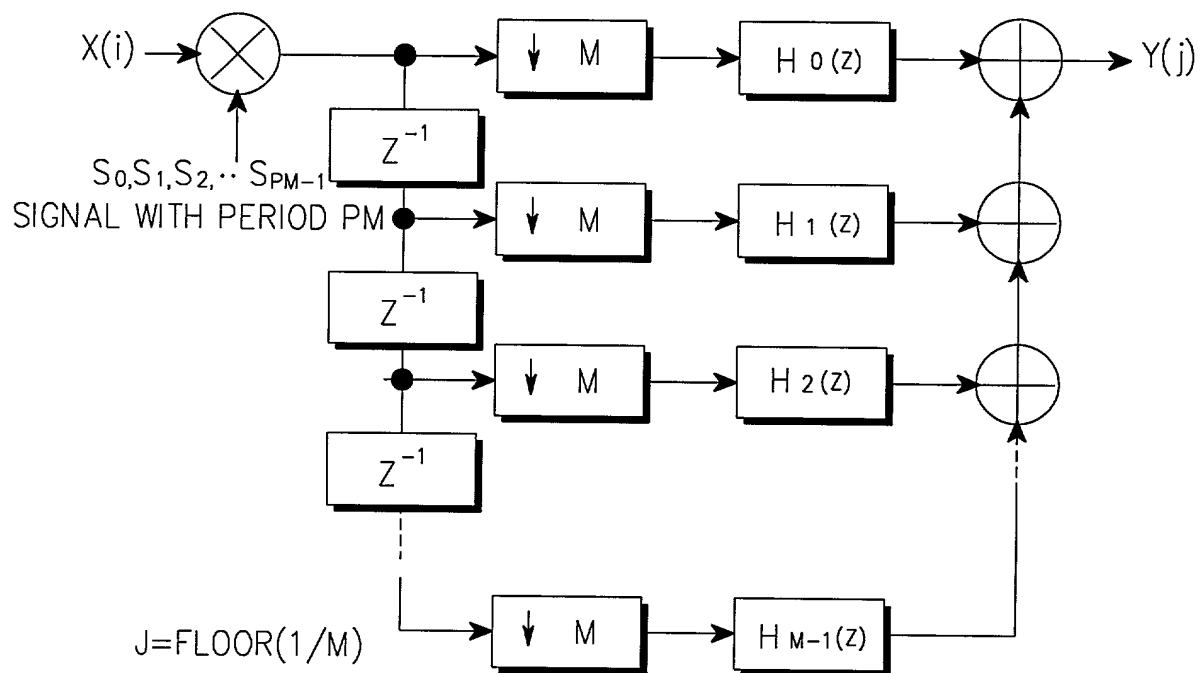


FIG. 9



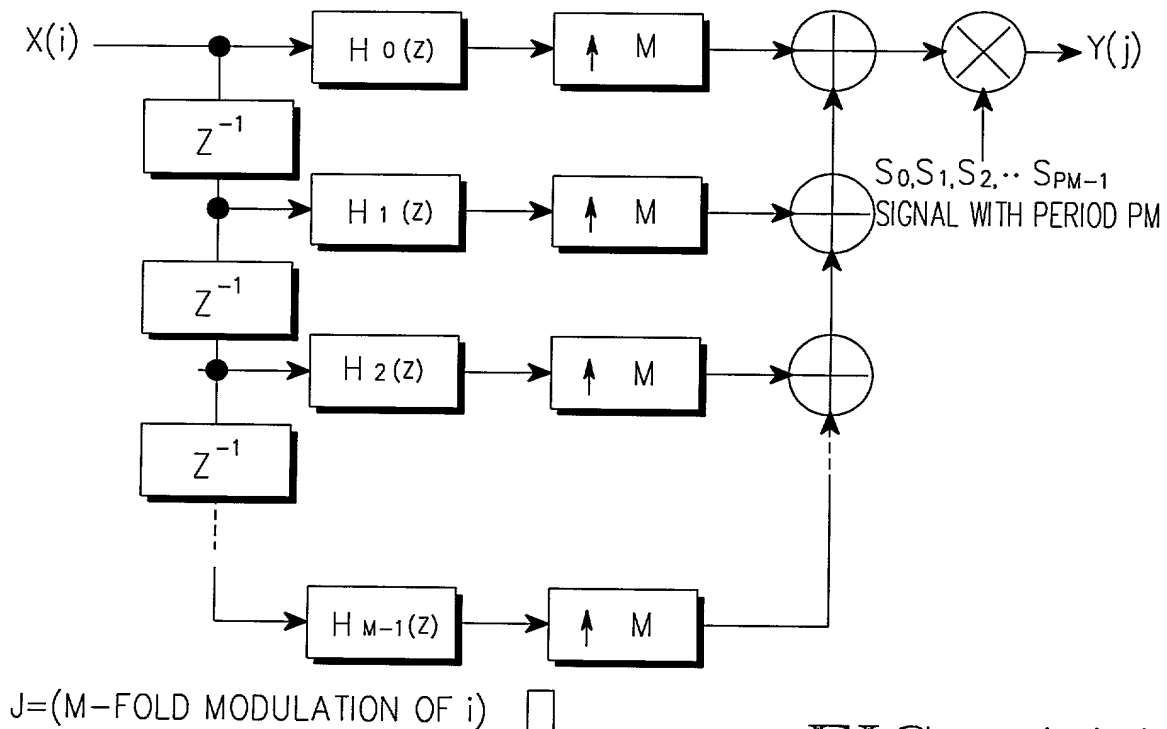
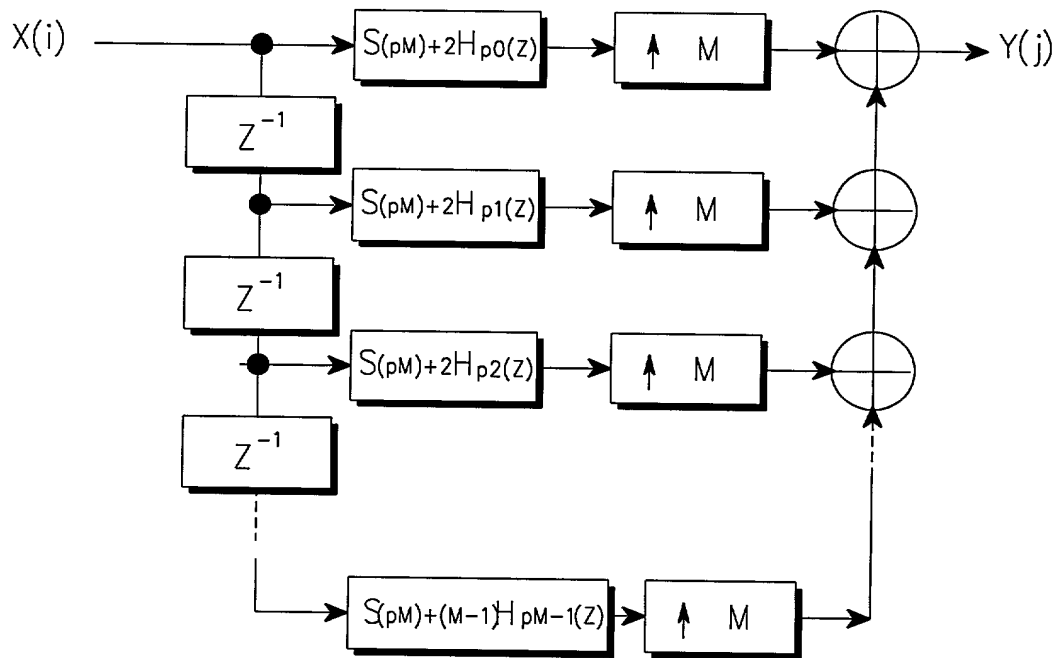


FIG. 11A



$P = \{\text{FLOOR}(1/M)\} \text{MOD } P$   
 $J = (M\text{-FOLD MODULATION OF } i)$

FIG. 11B

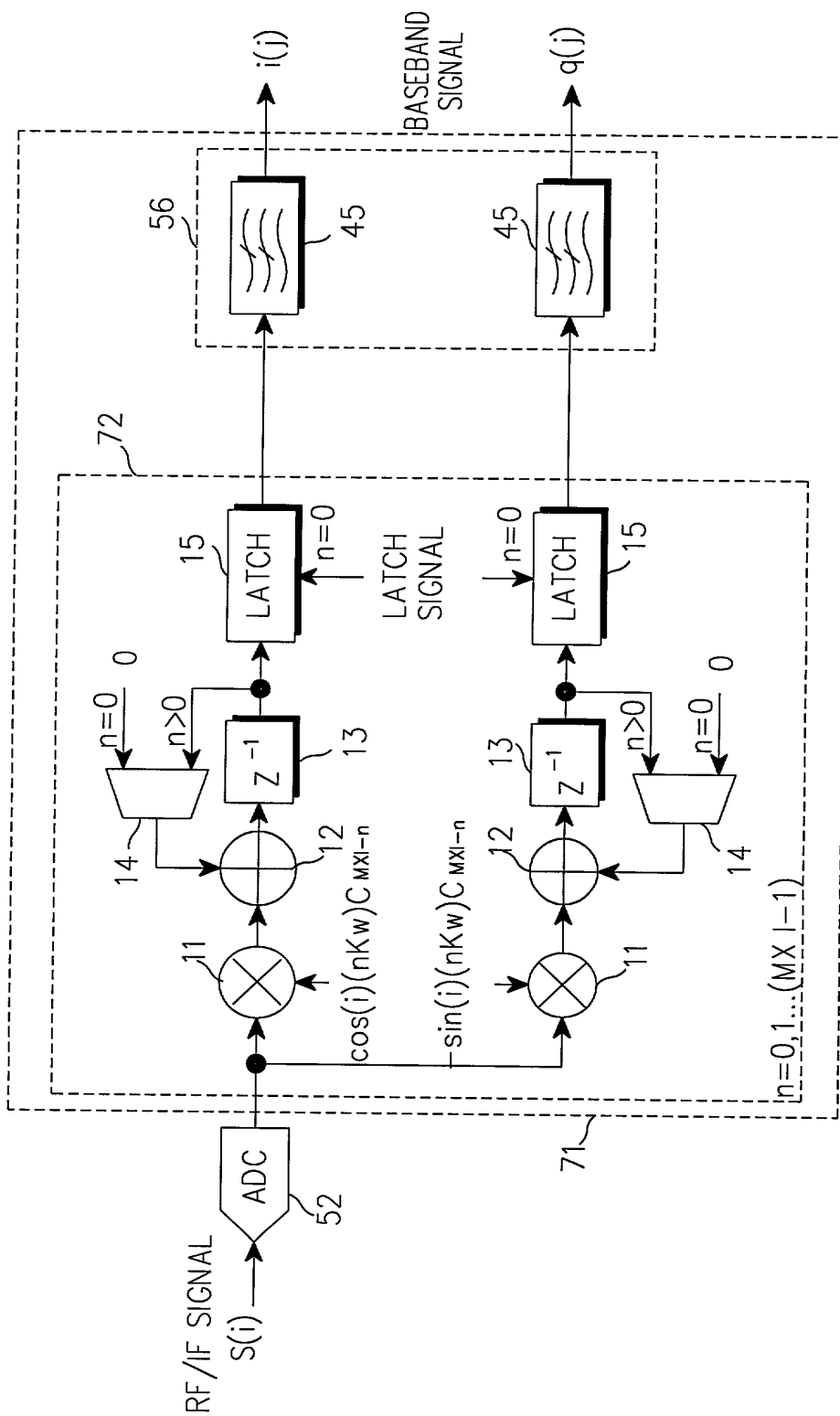


FIG.12

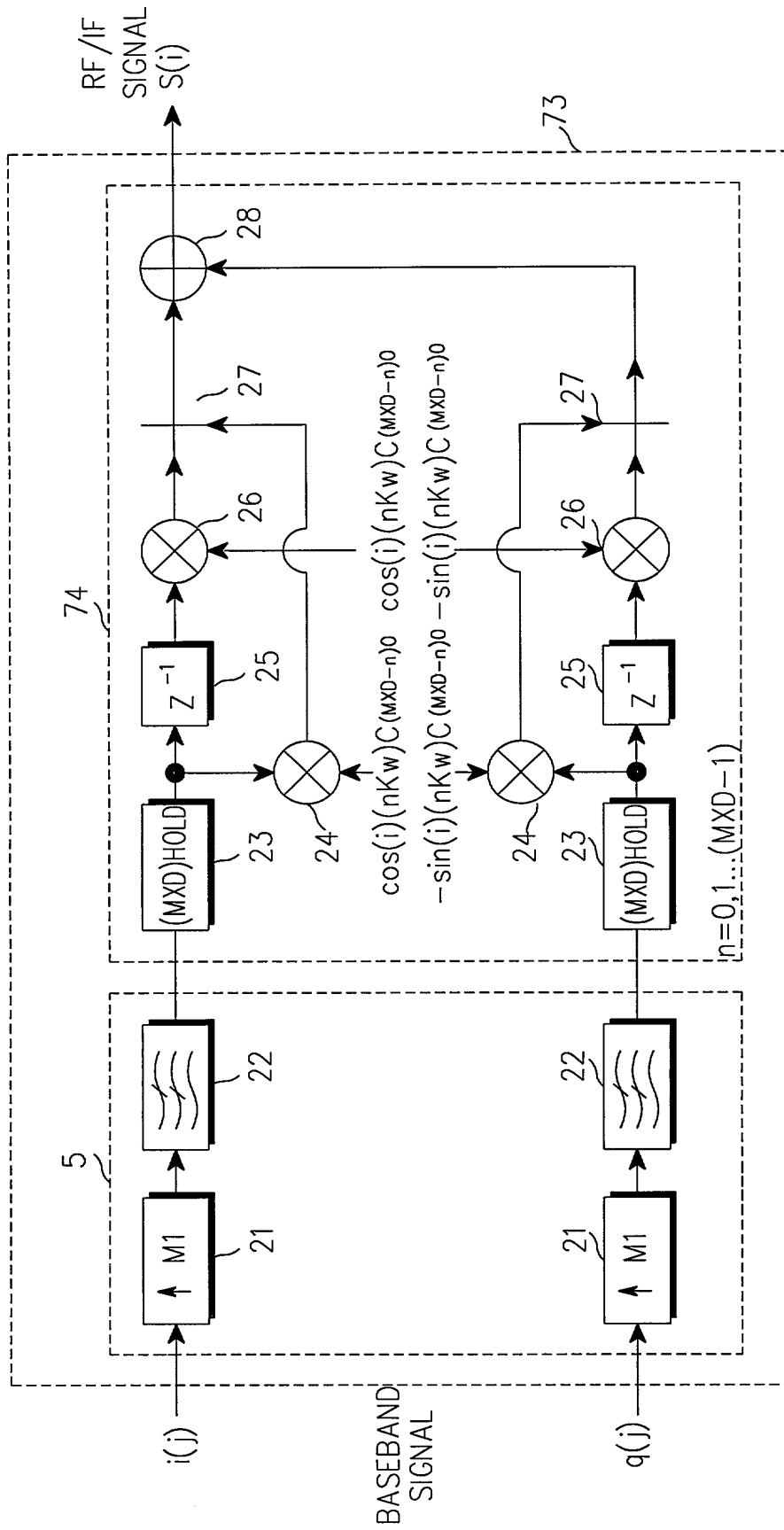


FIG.13